What is claimed is:

1. A method for fabricating trench isolations, comprising:

(a) providing a substrate with a trench therein;

(b) forming a first dielectric layer on the substrate and filling in the trench by low pressure chemical vapor deposition (LPCVD);

(c) etching the first dielectric layer to lower its surface to the opening of the trench; and

(d) forming a second dielectric layer on the first dielectric layer and filling the trench to form a trench isolation by high density plasma chemical vapor deposition (HDPCVD);

2. The method as claimed in claim 1, wherein step (a) further comprises steps of:

providing the substrate with a pad layer thereon;

defining a pattern on the pad layer;

etching the trench in the substrate using the pattern as a mask;

forming an oxide liner on the bottom and sidewalls of the trench by thermal oxidation; and

forming a nitride liner conformally on the pad layer and the oxide liner.

3. The method as claimed in claim 2, wherein the pad layer comprises a pad oxide layer and a pad nitride layer overlying the pad oxide layer.

4. The method as claimed in claim 1, wherein the aspect ratio of the trench exceeds 6.

5. The method as claimed in claim 1, wherein the first dielectric layer is TEOS.

6. The method as claimed in claim 5, wherein the thickness of the first dielectric layer is about 800~3500Å.

7. The method as claimed in claim 1, wherein the etching is performed by anisotropic etching and wet etching using hydrogen fluoride in order.

8. The method as claimed in claim 1, wherein the first dielectric layer is lowered about 100~1000Å, by etching, to the opening of the trench.

9. The method as claimed in claim 1, wherein HDPCVD is performed with a relatively low deposition/sputtering ratio and a relatively high deposition/sputtering ratio in order.

10. The method as claimed in claim 1, wherein the second dielectric layer is a silicon dioxide layer.

11. The method as claimed in claim 1, wherein the thickness of the second dielectric layer is about 2500~10000Å.

12. The method as claimed in claim 1, further comprising, after HDPCVD, planarizing the dielectric layer and the pad layer.

13. The method as claimed in claim 12, wherein the planarizing is performed by CMP.

14. The method as claimed in claim 13, wherein the CMP includes slurry-based CMP or fixed abrasive CMP.

15. The method as claimed in claim 13, further comprising, after CMP, performing a rapid thermal annealing procedure.

16. A method for fabricating trench isolations, comprising:

(a) providing a substrate with a first trench with a relatively high aspect ratio and a second trench with a relatively low aspect ratio therein;

(b) forming a first dielectric layer on the substrate and filling the trench by LPCVD;

(c) lowering the surface of the first dielectric layer to the openings of the both trenches by etching, wherein the first dielectric layer forms a spacer on the sidewalls of the second trench; and

(d) forming a second dielectric layer on the first dielectric layer and filling both trenches to form trench isolations by HDPCVD;

17. The method as claimed in claim 16, wherein step (a) further comprises steps of:

providing the substrate with a pad layer thereon;

defining a pattern on the pad layer;

etching a first trench with a relatively high aspect ratio and a second trench with a relatively low aspect ratio in the substrate using the pattern as a mask;

forming an oxide liner on the bottom and sidewalls of both trenches by thermal oxidation; and

forming a nitride liner conformally on the pad layer and the oxide liner.

18. The method as claimed in claim 17, wherein the pad layer comprises a pad oxide layer and the pad nitride layer overlying the pad oxide layer.

19. The method as claimed in claim 16, wherein the first dielectric layer is TEOS.

20. The method as claimed in claim 19, wherein the thickness of the first dielectric layer is about 500~3500Å.

21. The method as claimed in claim 16, wherein the etching is performed by anisotropic etching and wet etching using hydrogen fluoride in order.

22. The method as claimed in claim 16, wherein the first dielectric layer is lowered about 100~1000Å, by etching, to the opening of the trench.

23. The method as claimed in claim 16, wherein the HDPCVD is performed with a relatively low deposition/sputtering ratio and a relatively high deposition/sputtering ratio in order.

24. The method as claimed in claim 16, wherein the second dielectric layer is a silicon dioxide layer.

25. The method as claimed in claim 16, wherein the thickness of the second dielectric layer is about 2500~10000Å.

26. The method as claimed in claim 16, further comprising, after HDPCVD, planarizing the dielectric layer and the pad layer.

27. The method as claimed in claim 26, wherein the planarizing is performed by CMP.

28. The method as claimed in claim 27, wherein the CMP includes slurry-based CMP or fixed abrasive CMP.

29. The method as claimed in claim 27, further comprising, after CMP, performing a rapid thermal annealing procedure.